

FORM PTO-1449

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.
IMEC218.001AUSAPPLICATION NO.
09/935,789SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT
BY APPLICANT

(SEE SEVERAL SHEETS IF NECESSARY)

APPLICANT
Cathoor, et al.FILING DATE
August 22, 2001GROUP
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
	1	5,202,975	04/13/93	Rasbold et al.			
	2	5,327,561	07/05/94	Choi et al.			
	3	5,594,864	01/1997	Trauben	714	39	
	4	5,664,193	09/1997	Tirumalai	717	153	
	5	5,742,814	04/21/98	Balasa et al.			
	6	5,930,510	07/27/99	Beylin et al.			
	7	5,978,509	11/1999	Nachtergaele et al.	382	236	
	8	6,064,819	05/2000	Franssen et al.	717	156	
	9	6,078,745	06/2000	De Greef et al.	717	151	
	10	6,151,705	11/21/00	Santhanam			

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EXAMINER INITIAL		OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)
	11	Al-Furiah et al., "Memory Hierarchy Management for Interactive graph Structures", Proceedings, IEEE International Symposium on Parallel and Distributed Processing, March-April, 1998.
	12	Al-Mouhamed, M., et al., "A Heuristic Storage for Minimizing Access Time of Arbitrary Data Patterns", <i>IEEE Transactions on Parallel and Distributed Systems</i> , Vol. 8 No. 4, April 1997.
	13	Balasa, F., et al., "Dataflow-Driven Memory Allocation for Multi-Dimensional Signal Processing Systems", <i>Proceedings IEEE International Conference on Computer Aided Design, San Jose, CA</i> , pps. 31-34, Nov. 1994.
	14	Cathoor et al. "Global Communication and Memory Optimizing Transformations for Low Power Signal Processing Systems", IEEE workshop on VLSI signal processing, 1994.
	15	Cathoor et al., "System-Level Data-Flow Transformations for Power Reduction in Image and Video Processing", Proceedings of the Third IEEE International Conference on Electronics, Circuits and Systems, 1996.
	16	Cathoor, "Power-Efficient Data Storage and Transfer Methodologies: Current Solutions and Remaining Problems", IEEE Computer Society Workshop on VLSI System Level Design, 1998.
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	18	Danckaert et al., "System Level Memory Optimization for Hardware-Software Co-Design", Proceedings of the Fifth International Workshop on Hardware/Software Co-Design, 1997.
	19	De Greef, E., et al. "Mapping Real-Time Motion Estimation Type Algorithms to Memory Efficient, Programmable Multi-Processor Architectures", <i>Microprocessing and Microprogramming</i> , 41(5): 409-423, October 1995.
	20	De Greef, E., F. Cathoor, H. De Man, "Memory Size Reduction Through Storage Order Optimization for Embedded Parallel Multimedia Applications", International Parallel Processing Symposium (IPPS) In Proceedings Workshop on Parallel Processing and Multimedia Geneva, Switzerland, pp. 84-98, April 1997.
	21	Diquet et al., "Formalized Methodology for Data Reuse Exploration in Hierarchical Memory Mappings", "International Symposium on Low Power Electronics and Design (IEEE Cat. No. 97TH8332), pp. 30-35, August 1997.

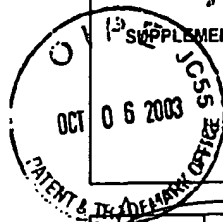
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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT (USE SEVERAL SHEETS IF NECESSARY)		RECEIVED OCT 8 2003	
		APPLICANT Cathoor, et al.	GROUP 2151
		FILING DATE August 22, 2001	Technology Center 2100



EXAMINER INITIAL	OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)
22	Fang, J., et al., "An Iteration Partition Approach for Cache or Local Memory Thrashing on Parallel Processing", IEEE Transactions on Computers, Vol. C-42, No 5, pp. 529-546, May 1993.
23	Franssen et al., "Control Flow Optimization for Fast System Simulation and Storage Minimization", European Design and Test Conference, 1994.
24	Li, YanBing et al., "A Task-Level Hierarchical Memory Model for System Synthesis of Multiprocessors", Proceedings, 34 th Design Automation Conference, June 1997.
25	Lippens, P., et al., "Allocation of Multiport Memories for Hierarchical Data Streams", Proceedings IEEE International Conference on Computer Aided Designs, pps. 728-735, Santa Clara, Nov. 1993.
26	Moolenaar, et al., "System-Level Power Exploration for MPEG-2 Decoder on Embedded Cores: A Systematic Approach", 1997 IEEE Workshop on Signal Processing Systems, 1997.
27	Nachtergaele, L., F. Cathoor, F. Balasa, F. Franssen, E. De Greef, H. Samsom, H. De Man, "Optimization of Memory Organization and Hierarchy for Decreased Size and Power in Video and Image Processing Systems", Proceedings International Workshop on Memory Technology, Design and Testing, San Jose, CA, pp. 82-87, August 1995.
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32	Stok, L., "Data Path Synthesis", The VLSI Journal, Vol. 18, pp. 1-71, June 1994.
33	Verhaegh, W., et al., "Improved Force-Directed Scheduling in High-Throughput Digital Signal Processing", IEEE Transactions on CAD and Systems, Vol. 14, No. 8, pps. 945-960, Aug. 1995.
34	Wuytack, S., et al., "Flow Graph Balancing for Minimizing the Required Memory Bandwidth", IEEE System Synthesis, 1996 Proceedings, 9 th edition, 1996.
35	Wuytack, S., F. Cathoor, L. Nachtergaele, H. De Man, "Power Exploration for Data Dominated Video Applications, Proceedings IEEE International Symposium on Low Power Design", Monterey, pp. 359-364, August 1996.

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